#16 DAC 15

PTO/SB/64 (10/01)
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PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNINTENTIONALLY UNDER 37 CFR 1.137(b)	Docket Number (Optional) 061607-1100

First Named Inventor: **Louis F. Villarosa, Jr. et al.**

Application No.: **09/353,120** Group Art Unit: **2631**

Filed: **Circuit and Method for Detecting and Correcting Data Clocking Errors** Examiner: **Kumar, P.**

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at (703) 305-9282.

The above-identified application became abandoned for failure to file a timely and proper reply to a notice or action by the Untied States Patent and Trademark Office. The date of abandonment is the day after the expiration date of the period set for reply in the Office notice or action plus extensions of time actually obtained.

APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION

NOTE: A grantable petition requires the following items:
(1) Petition fee;
(2) Reply and/or issue fee;
(3) Terminal disclaimer with disclaimer fee – required for all utility and patent applications filed before June 8, 1995, and for all design applications; and
(4) Statement that the entire delay was unintentional.

1. Petition Fee

☐ Small entity – fee $**665.00** (37 C.F.R. 1.17(m)). Applicant claims small entity status. See 37 CFR 1.27.

☒ Other than small entity – fee $**1,330.00** (37 C.F.R. 1.17(m))

2. Reply and/or fee

A. The reply and/or fee to the above-noted Office action in the form of _____ (identify type of reply):
☐ has been filed previously on _____.
☒ is enclosed herewith.

B. The issue fee of $
☐ has been paid previously on _____.
☐ is enclosed herewith.

03/02/2004 AWONDAF1 00000027 09353120

02 FC:1453 1330.00 DA

3. **Terminal disclaimer with disclaimer fee**

☒ Since this utility/plant application was filed on or after June 8, 1995, no terminal disclaimer is required.

☐ A terminal disclaimer (and disclaimer fee (37 CFR 1.20(d) of $55.00 for a small entity or $110.00 for other than a small entity) disclaiming the required period of time is enclosed herewith (see PTO/SB/63).

4. **Statement.** The entire delay in filing the required reply from the due date for the reply until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional. [NOTE. The united States Patent and Trademark Office may require additional information if there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137(b) was unintentional (MPEP 711.03(c), subsections (III)(C) and (D))].

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

02/25/04
Date

Signature

Telephone Number: (770) 933-9500

Scott A. Horstemeyer, Reg. No. 34,183
Typed or printed name

Thomas, Kayden, Horstemeyer & Risley LLP
100 Galleria Parkway
Suite 1750
Atlanta, GA 30339

Enclosures:

☒ Fee Payment
☒ Reply
☐ Terminal Disclaimer Form
☐ Additional sheets containing statements establishing unintentional delay
☒ Other: **Petition Under 37 C.F.R. 1.137(b) Statement of Unintentional Delay**

CERTIFICATE OF MAILING [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

☒ deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

☐ transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703) 308-6916.

February 25, 2004
Date

Evelyn Sanders
Signature

Evelyn Sanders
Typed or printed name

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

App. No.:	09/353,120	Art Unit:	2631
Applicant:	Louis F. Villarosa, Jr. *et al.*	Examiner:	Kumar, P.
Filed:	July 14, 1999	Confirmation No.:	3012
Title:	CIRCUIT AND METHOD FOR DETECTING AND CORRECTING DATA CLOCKING ERRORS	Docket No.:	061607-1100

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION UNDER 37 C.F.R. §1.137(b)
STATEMENT OF UNINTENTIONAL DELAY

Sir:

We hereby petition to revive the above-identified application from abandonment in accordance with 37 C.F.R. §1.137(b). We also wish to state that the delay in reply was unintentional.

We received from the United States Patent and Trademark Office (USPTO) a Final Rejection, mailed April 23, 2003 (Paper No. 15). In response thereto, we submitted to the USPTO an After-Final Response (See Appendix A) with a certificate of mailing date of June 19, 2003, which was less than two months after the mailing date of the Final Rejection, thereby extending the statutory period to the mailing date of an Advisory Action. Shortly after filing the After-Final Response, we received a return postcard from the USPTO showing receipt of the After-Final Response (See Appendix B).

At that time, we were under the assumption that the USPTO would reply to our After-Final Response and we waited for such a reply. However, as we later discovered, the After-Final Response that we filed had been misplaced at the USPTO and of course was not acted upon by the Examiner.

While waiting for a reply from the USPTO, we unintentionally let the six month statutory period expire, having expired on October 23, 2003. At this time, having still not received any action from the USPTO, we called the Examiner to inquire about the status of the file. We then discovered that the After-Final Response had not been entered and we therefore re-submitted the Response for the Examiner's review.

On February 24, 2004, we were informed that the Examiner reviewed the re-submitted After-Final Response and was preparing an Advisory Action to indicate that the Response would not be entered and that the application would not be allowed. Therefore, having unintentionally waited beyond the six month statutory period for a reply from the USPTO, we hereby submit this petition to revive the application from abandonment. Also, we wish to enter a Request for Continued Examination (RCE) in order that the Response might be entered.

Respectfully submitted,

Scott A. Horstemeyer
Reg. No. 34,183

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.
Suite 1750
100 Galleria Parkway N.W.
Atlanta, Georgia 30339
(770) 933-9500

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 25, 2004.

Evelyn Sanders
Signature – Evelyn Sanders

Enclosures

APPENDIX A

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to:

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Alexandria, Virginia 22313-1450

on 6-19-03.

Evelyn Sanders
Evelyn Sanders

In re application of: Louis F Villarosa, Jr. et al.

Group No.: 2631

Serial Number: 09/353,120

Examiner: Kumar, P.

Filing Date: July 14, 1999

Title: **CIRCUIT AND METHOD FOR DETECTING AND CORRECTING DATA CLOCKING ERRORS**

Attached are the following documents for filing with the USPTO:

Return Postcard
Amendment Transmittal Letter
Fourth Response (With Amendments)

In re **PATENT** application of:

Louis F. Villarosa, Jr., *et al.*

Examiner: Kumar, P.

Serial No: **09/353,120**

Group No.: 2631

Filed: **July 14, 1999**

Docket No.: 061607-1100

Title: **CIRCUIT AND METHOD FOR DETECTING AND CORRECTING DATA CLOCKING ERRORS**

Confirmation No.: 3012

AMENDMENT TRANSMITTAL LETTER

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Transmitted herewith is an amendment in the above-identified application.

- ☒ Response/Amendment
- ☐ Fee as Calculated Below
- ☒ No additional fee is required.
- ☐ Small Entity status has been established.
- ☐ Terminal Disclaimer
- ☐ Corrected Drawings
- ☐ Other:

CLAIMS AS AMENDED FOR LARGE ENTITY					
	Claims After Amendment	Highest Prev. Paid For	Extra	Rate	Additional Fee
Total Claims	22	- 26	0	x $18.00	= $0
Independent Claims	3	- 3	0	x $42.00	= $0
Total Additional Fee for this Amendment					**= $0**

- ☐ A check in the amount of $ is enclosed.
- ☐ A Credit Card Payment Form PTO-2038 is attached in the amount of $.
- ☐ The Commissioner is hereby authorized to charge to our Deposit Account No. the amount of $ for the fee identified above. A duplicate of this Amendment Transmittal Letter is included herewith.
- ☒ The Commissioner is authorized to charge any insufficiencies, and the Commissioner is hereby requested to credit any overpayments to our Deposit Account No. 16-0255.

Customer No.: 24504

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

Date: 6/19/03

Glenn W. Brown

Glenn W. Brown, Reg. No. 51,310
Attorney for Applicant(s)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Villarosa *et al.*

Group Art Unit: 2631

Serial No.: **09/353,120**

Examiner: Kumar, P.

Filed: July 14, 1999

Docket No. 061607-1100

For: CIRCUIT AND METHOD FOR DETECTING AND CORRECTING DATA CLOCKING ERRORS

FOURTH RESPONSE (WITH AMENDMENTS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The outstanding final Office Action mailed ***April 23, 2003*** (Paper No. 15) has been carefully considered. In response thereto, please enter the following amendments in which claims 1 and 11 are amended. Claims 1-7, 10-16, 19-22, 25, and 27-29 are now pending in the present application. Reconsideration and allowance of the application and presently pending claims, as amended, are respectfully requested.

AUTHORIZATION TO DEBIT ACCOUNT

It is believed that no extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to deposit account no. 16-0255.

AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated hereafter.

Claims:

1. (Currently Amended) A circuit for detecting clocking errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a clock generating circuit configured to generate a master clock signal, a DCE clocking signal, and an internal clocking signal, each of the DCE clocking signal and internal clocking signal having a first frequency that is a fraction of the frequency of the master clock signal;

a sample enable generator configured to receive the master clock signal and the internal clocking signal and to generate a first sample enable signal at a first time and a second sample enable signal at a second time, the second time being subsequent to the first time; and

a sample comparator having inputs that receive said first sample enable signal, said second enable signal and said DTE data signal, the sample comparator configured to sample the DTE data signal at the first time and sample the DTE data signal at the second time, the sample comparator further configured to compare the DTE data signal sampled at the first time with the DTE data signal sampled at the second time and determine, from the comparison, whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

2. (Original) The circuit of claim 1, wherein the frequency of said master clocking signal is approximately 8 times the frequency of said DCE clocking signal.

3. (Original) The circuit of claim 1, wherein the time interval between said first time and said second time is approximately 1/8 of the period of said DCE clocking signal.

4. (Previously Amended) The circuit of claim 1, wherein said sample comparator generates a selector control signal when the sample comparator determines that the DTE data signal has undergone a transition.

5. (Previously Amended) The circuit of claim 4, wherein the clock generating circuit comprises:

a clock generator that generates the DCE clocking signal;

an inverter that produces an inverted DCE clocking signal from the DCE clocking signal; and

a selector that receives the DCE clocking signal and the inverted DCE clocking signal and produces the internal clocking signal that is selected, in response to the selector control signal, from the group consisting of the DCE clocking signal and the inverted DCE clocking signal.

6. (Previously Amended) A circuit for detecting and correcting clocking errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

means for producing a master clock signal;

means for deriving a DCE clocking signal and an internal clocking signal from said master clock signal, said internal clocking signal having the same frequency as the DCE clocking signal;

means for obtaining a first sample of said DTE data signal at a first time and obtaining a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal;

means for comparing said first sample to said second sample;

means for generating a selector control signal if said first sample is different from said second sample;

means for inverting said internal clocking signal to produce an inverted clocking signal; and

means for selecting, in response to said selector control signal, an output signal from the group consisting of said internal clocking signal and said inverted clocking signal.

7. (Original) The circuit of claim 6, wherein the interval between said first time and said second time is approximately 1/8 of the period of the DCE clocking signal.

8. (Cancelled)

9. (Cancelled)

10. (Previously Amended) The circuit of claim 6, further comprising:

means for latching said DTE data signal, the means for latching being clocked by said internal clocking signal.

11. (Currently Amended) A method for detecting clocking errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

providing a master clock signal;

deriving a DCE clocking signal and an internal clocking signal from said master clock signal, said internal clocking signal ~~having the same frequency as the~~and said DCE clocking signal having a first frequency that is a fraction of the frequency of the master clock signal;

obtaining a first sample of said DTE data signal at a first time and a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the time interval between said first time and said second time being less than the period of the DCE clocking signal;

comparing said first sample to said second sample; and

determining whether the DTE data signal has undergone a transition during the time interval between the first time and the second time.

12. (Original) The method of claim 11, wherein the interval between said first time and said second time is approximately 1/8 of the period of the DCE clocking signal.

13. (Original) The method of claim 11, further comprising the step of:

generating a selector control signal if said first sample is different from said second sample.

14. (Previously Amended) The method of claim 13, further comprising the steps of:

inverting said DCE clocking signal to produce an inverted clocking signal; and

producing said internal clocking signal that is selected, in response to said selector control signal, from the group consisting of said DCE clocking signal and said inverted clocking signal.

15. (Previously Amended) The method of claim 14, further comprising the step of:

latching said DTE data signal.

16. (Previously Amended) The circuit of claim 5, further comprising:

a data latch, clocked by said internal clocking signal, for latching said DTE data signal.

17. (Cancelled)

18. (Cancelled)

19. (Previously Amended) The circuit of claim 16, wherein said first enable signal is generated on the rising edge of said output signal and said second enable signal is generated an integral number of master clock signals after said first enable signal.

20. (Previously Amended) The circuit of claim 16, wherein said first enable signal is generated one master clock period before the rising edge of said internal clocking signal and said second enable signal is generated one master clock period after the rising edge of said internal clocking signal.

21. (Previously Amended) The circuit of claim 28, wherein said first enable signal is generated on the rising edge of said internal clocking signal and said second enable signal is generated an integral number of master clock signals after said first enable signal.

22. (Previously Amended) The circuit of claim 28, wherein said first enable signal is generated one master clock period before the rising edge of said internal clocking signal and said second enable signal is generated one master clock period after the rising edge of said internal clocking signal.

23. (Cancelled)

24. (Cancelled)

25. (Previously Amended) The method of claim 15, further comprising the step of:

performing said obtaining step and said latching step according to a time sequence referenced to said internal clocking signal.

26. (Cancelled)

27. (Previously Added) The circuit of claim 4, wherein the clock generating circuit comprises:

a clock generator that generates said internal clocking signal;

an inverter that produces an inverted clocking signal from the internal clocking signal; and

a selector that receives the internal clocking signal and the inverted clocking signal and produces the DCE clocking signal that is selected, in response to the selector control signal, from the group consisting of the internal clocking signal and the inverted clocking signal.

28. (Previously Added) The circuit of claim 27, further comprising:

a data latch, clocked by said internal clocking signal, for latching said DTE data signal.

29. (Previously Added) The method of claim 13, further comprising the steps of:

inverting said internal clocking signal to produce an inverted clocking signal; and

producing said DCE clocking signal that is selected, in response to said selector control signal, from the group consisting of said internal clocking signal and said inverted clocking signal.

REMARKS

Applicants wish to express their sincere appreciation for the Examiner's indication of allowable subject matter in which claims 1-7, 10, 16, 19-22, 27, and 28 have been allowed. Claim 1 has been amended to correct a minor informality and claim 11 has been amended to incorporate subject matter of claim 1 that the Examiner indicated as allowable.

Response to 35 U.S.C. §102 Rejection

Claims 11-13 stand rejected under 35 U.S.C. §102(b) as being anticipated by *Hedberg* (U.S. Patent No. 5,526,361). Applicants respectfully traverse this rejection because claim 11, as amended, includes steps that are not disclosed in *Hedberg*.

Claim 11 has been amended to include steps that are similar to the functions of the allowable claim elements of claim 1. For example, claim 11 now includes ***"said internal clocking signal and said DCE clocking signal having a first frequency that is a fraction of the frequency of the master clock signal."*** *Hedberg* does not teach or suggest signals derived from a master clock signal, the derived signals having a frequency that is a fraction of the frequency of the master clock signal. Instead, *Hedberg* appears to teach that the frequency of all phase-shifted signals are the same as that of CK_{in}.

Anticipation requires identity of the claimed process and a process of the prior art. The claimed process, including each step thereof, must have been described or embodied, either expressly or inherently, in a single reference. *See, e.g., Glaverbel S.A. v. Northlake Mkt'g & Supp., Inc.,* 45 F.3d 1550, 33 USPQ 2d 1496 (Fed. Cir. 1995). Since *Hedberg* does not embody the deriving of a DCE clocking signal and an internal clocking signal "having a first frequency that is a fraction of the frequency of the master clock signal," it is respectfully requested that the 35 U.S.C. §102(b) rejection be withdrawn.

Dependent claims 12 and 13 are believed to be allowable for at least the reason that these claims depend from allowable independent claim 11. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Response to 35 U.S.C. §103 Rejection

Claims 14, 15, 25, and 29 stand rejected under 35 U.S.C. §103 as allegedly being unpatentable over *Hedberg*. Applicants respectfully traverse this rejection since *Hedberg* fails to teach deriving an internal clocking signal and DCE clocking signal having ***"a first frequency that is a fraction of the frequency of the master clock signal"*** as mentioned above. Furthermore, *Hedberg* does not suggest any motivation to modify the frequencies of the phase-shifted signals nor is there any motivation taught in the prior art to modify the frequency of *Hedberg*'s phase-shifted signals. For at least these reasons, it is respectfully requested that the Examiner kindly withdraw the 35 U.S.C. §103 rejection.

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all rejections have been traversed, and that the pending claims 1-7, 10-16, 19-22, 25, and 27-29 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned agent at (770) 933-9500.

Respectfully submitted,

Glenn W. Brown
Reg. No. 51,310

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.
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100 Galleria Parkway N.W.
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 19, 2003.

Evelyn Sanders
Signature -

APPENDIX B

Serial No.: 09/353,120 Filed: July 14, 1999
Patent No.: Issued:
Applicant: Louis F. Villarosa, Jr., et al.
Title: Circuit and Method for Detecting and Correcting Data Clocking Errors
Docket No.: 061607-1100 C/M Date: 06/19/2003
EM No.: Due Date: 07/23/03

PATENT AND TRADEMARK OFFICE STAMP HEREON ACKNOWLEDGES RECEIPT OF THE BELOW IDENTIFIED PAPERS:

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OIPE JC48 JUN 23 2003 PATENT & TRADEMARK OFFICE

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☐ Certificate of Correction x 2
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☐ in duplicate

Person Mailing: ETS

Responsible Atty: SAH/GWB